Verification of Industrial Designs Using A Computing Grid With More than 100 Nodes

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Summary of Presentation

Formal verification, especially error detection, is rapidly increasing in importance with the rising complexity of designs. The main constraint in verification is the total amount of resources available - both time as well as memory. Most attempts at verification only use a single processor. Recently, various attempts have been made to use parallel and distributed methods for verification.

However, verification in a Grid-based environment has not yet been very widely adopted. As personal computers gain in computing capacity, the concept of computation grids is gaining acceptance. Here, a grid is a network of machines that may not be dedicated to a specific computational use, but may only be available some of the time. This is a unique environment where massive parallelism is possible by using otherwise idle CPU cycles from a large number of computers. Such processors may even be in geographically diverse locations. We describe a Grid-based verification environment for detecting errors in a design. We verify user-written assertions as well as properties, e.g. unreachable code, index-out-of-range, that are extracted automatically from the design using a state-of-the-art HDL parser. Such an approach can help the user to quickly find RTL level bugs earlier in the design cycle.

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In an industrial setting, due to availability of a large number of machines, bounded model checking can be efficiently performed using a distributed Grid-based computing environment as we describe in our presentation. We also discuss the experiences in application of an in-house property verifier using state-of-the-art frontend to the verification of various industrial properties.

We explore parallelization of both BMC and BDD based model checking using state space partitioning[1]. In this scheme, all processors work independently of each other, thus it is suitable for scaling verification to a grid-like network.

References

[1] Subramanian Iyer, Jawahar Jain, Mukul Prasad, Debashis Sahoo, and Tom Sidle. Error detection using BMC in a parallel environment. In Dominique Borrione and Wolfgang Paul, editors, *CHARME*, Lecture Notes in Computer Science. Springer, 2005.

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